

REMARKS

Claims 1-2, 4, 6-7 and 10-11 are pending in this application, of which claim 1 has been amended. Claims 3, 5, 8-9 and 12-31 have been canceled. No new claims have been added.

Claims 1-2 and 4 stand rejected under 35 U.S.C. § 103(a) as unpatentable over **Eldridge et al.**

Applicants respectfully traverse this rejection.

As noted in Applicants' response of January 27, 2006, FIG. 33 of **Eldridge et al.** clearly shows that decoupling capacitor 3370 is not entirely embedded in substrate 3320 because it is not covered on its top surface by the substrate, in contrast to the present invention, in which embedded capacitor 20 is entirely covered on its top surface by the build-up interconnection layer 14, as shown in FIG. 4.

More specifically, in FIG. 33, the capacitor is provided in a depression formed in a build-up substrate and there is formed a gap between the capacitor and the sidewall or bottom surface of the depression, in which the capacitor is provided. Thus, the capacitor of **Eldridge et al.** is not enclosed or surrounded "closely", in contrast to the meaning of the word "embed."

According to Webster's New World Dictionary, Third College Edition, "embed" means to "set or fix firmly in a surrounding mass." Clearly, the capacitor of **Eldridge et al.** is not set or fixed firmly in a surrounding mass.

Thus, contrary to the disclosure of **Eldridge et al.**, the capacitor of the present invention fully meets the dictionary definition of "embedded."

In response to this argument, the Examiner states:

In reviewing Eldrige et al., the examiner believes the capacitor 3370 is set firmly around multi-layer substrate 3320. The applicants are correct that there is a gap between the substrate and capacitor but that does not mean that it is not firmly set. Based on the definition given by the applicants, the examiner is taking the position that a device could be surrounded by a mass but it does not mean that it is connected to that mass from all sides (Sic).

Accordingly, claim 1 has been amended to recite that the capacitor is “embedded entirely within said insulation layer such that its top, bottom and side surfaces are in contact with said resin insulation layer....”

Further, claim 1 has been amended to clarify the feature that said insulation layer is “located between a lower interconnection layer and an upper interconnection layer.” This amendment is supported on page 16, lines 28-31 of the specification.

This amendment clarifies the feature that an interconnection layer is formed further on the capacitor and that the capacitor is embedded entirely in the multilayer interconnection structure.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

Claims 10 and 11 have been allowed.

In view of the aforementioned amendments and accompanying remarks, claims 1-2, 4, 6-7 and 10-11, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants’ undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

U.S. Patent Application Serial No. **10/621,445**
Response to Office Action dated April 18, 2006

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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